REMARKS/ARGUMENTS

In the Office Action, the Examiner noted that claims 1-46 are pending in the application. The Examiner additionally stated that claims 1-46 are rejected. By this amendment, claims 17-31 have been cancelled and claims 1, 32-35, and 41-43 have been amended. Hence, claims 1-16 and 32-46 are pending in the application.

Applicant hereby requests further examination and reconsideration of the application, in view of the foregoing amendments.

In the Specification

Applicant has amended the specification to secure a substantial correspondence between the claims amended herein and the remainder of the specification. No new matter is presented.

In the Claims

Rejections Under 35 U.S.C. §102(b)

The Examiner rejected claims 1, 17, and 32 under 35 U.S.C. 102(b) as being anticipated by Mahalingaiah et al., U.S. Patent No. 6,389,512 (hereinafter, Mah). Applicant respectfully traverses the Examiner's rejections.

As per claim 1, the Examiner noted that Mahalingaiah teaches an apparatus in a pipeline microprocessor (i.e., 12 in Fig. 1), for ensuring coherency of instructions within stages of the pipeline microprocessor, the apparatus comprising:

- instruction cache management logic (i.e., combination of 40, 42, 44, 46, 48, and 50 in Fig. 2), configured to receive an address corresponding to a next instruction (i.e. the address corresponding to the instruction that has been fetched but not yet retired), and configured to detect that a part of a memory page corresponding to said next instruction cannot be freely accessed without checking for coherency of the instructions within said part of said memory page (i.e., addresses corresponding to memory locations being modified are compared to the addresses stored in the core snoop buffer on a page basis) and, upon detection, configured to provide said address; and

- synchronization logic (i.e., combination of 40, 42, 44, 46, 48, and 50 in Fig. 2), configured to receive said address from said instruction cache management logic, and configured to direct data cache management logic to check for coherency of the instructions within said part of said memory page, and, if the instructions are not coherent within said part of said memory page, said synchronization logic is configured to direct the pipeline microprocessor to stall a fetch of said next instruction until the stages of the pipeline microprocessor have executed all preceding instructions (i.e., if a match is detected, then instructions are flushed from the instruction processing pipeline and prefetched) (e.g., see the abstract and Figs. 1 and 2).

As per claims 17 and 32, The Examiner noted that Mah teaches a method and an apparatus in a pipeline microprocessor (i.e., 12 in Fig. 1), for ensuring coherency of instructions within stages of the pipeline microprocessor, the apparatus comprising:

- data cache management logic (i.e., combination of 40, 42, 44, 46, 48, and 50 in Fig. 2), configured to receive an address corresponding to a store instruction (i.e., the next instruction, the address corresponding to the instruction that has been fetched but not yet retired) that is pending, and configured to detect that a part of a memory page corresponding to said store instruction cannot be freely accessed without checking for coherency of the instructions within said part of said memory page (i.e., addresses corresponding to memory locations being modified are compared to the addresses stored in the core snoop buffer on a page basis) and, upon detection, configured to provide said address; and
- synchronization logic (i.e., combination of 40, 42, 44, 46, 48, 50 in Fig. 2), configured to receive said address from said data cache management logic, and configured to direct instruction cache management logic to check for coherency of the instructions within said part of said memory page, and, if the instructions are not coherent within said part of said memory page, said synchronization logic is configured to direct the pipeline microprocessor to stall a fetch of said store instruction until the stages of the pipeline microprocessor have executed all

preceding instructions (i.e., if a match is detected, then instructions are flushed from the instruction processing pipeline and prefetched) (e.g. see the abstract and Figs. 1 and 2).

Applicant respectfully disagrees with the Examiner's rejections of claims 1, 17, and 32, along the Examiner's characterization of Mah. More specifically, claim 1 recites, in combination with other elements and limitations, that the address received by the instruction cache management logic and provided to the synchronization logic corresponds to a next instruction *to be fetched.* Mah does not teach such a limitation. Rather, Mah teaches, as the Examiner has quoted above, the address which is used by Mah corresponds to an instruction *which has already been fetched and is operative in the pipeline.* Accordingly, Mah teaches a technique for discovering incoherency of instructions which have already been fetched from memory. Applicant's invention, in contrast, enables a microprocessor to stall operations in upper stages of a pipeline, *without requiring a flush of the pipeline,* when incoherency is detected. In other words, the check for incoherency is performed *prior to fetching of a next instruction from memory.*

Mah does not suggest or provide any other teaching that would motivate one skilled in the art to provide the apparatus recited in claim 1, as is argued above. Accordingly, Applicant respectfully requests that the rejection of claim 1 be withdrawn.

By this amendment, claim 17 has been cancelled, thereby rendering the rejection moot.

With regard to amended claim 32, it is recited that the detecting corresponds to a next instruction to be fetched and that if instructions are not coherent, stalling a fetch of the next instruction from the instruction cache until the stages of the pipeline microprocessor have executed all preceding instructions. As is noted above in traversal of the rejection of claim 1, Mah does not teach such a limitation. Rather, the address which is used by Mah corresponds to an instruction *which has already been fetched and is operative in the pipeline.* Thus, Mah teaches detecting incoherency of instructions which have already been fetched from memory, but does not teach, suggest, or allude to detecting incoherency prior to fetch of an instruction from an instruction cache. Since Mah does

not suggest or provide any other teaching that would motivate one skilled in the art to provide the limitations recited in claim 32, Applicant respectfully requests that the rejection be withdrawn.

In rejections of dependent claims under 35 U.S.C. 103, the Examiner argues that Mah in view of Kyker et al., U.S. Patent Application No. 2004/0015675 (hereinafter, Kyker), provides motivation to one skilled to utilize a plurality of part-page ownership bits (i.e., FINE HITS bits as noted in Kyker paragraph [0052]) to track coherency of instructions.

Rejections Under 35 U.S.C. §103(a)

The Examiner rejected claims 2-16, 18-31, and 33-46 under 35 U.S.C. 103(a) as being unpatentable over Mah in view of Kyker et al., U.S. Patent Application No. 2004/0015675 (hereinafter, Kyker). Applicant respectfully traverses the Examiner's rejections.

Since by this amendment, claims 17-31 have been cancelled, the corresponding rejections are moot.

With respect to claims 2-16 and 33-46, these claims depend from claims 1 and 32, respectively, and add further limitations over that subject matter which has been argued above to be allowable over Mah. In that Mah does not suggest the limitations of claims 1 and 32, Applicant respectfully requests that the Examiner withdraw the rejections of claims 2-16 and 33-46.

CONCLUSIONS

In view of the arguments advance above, Applicant respectfully submits that claims 1-16 and 32-46 are in condition for allowance. Reconsideration of the rejections is requested, and allowance of the claims is solicited.

Applicant earnestly requests that the Examiner contact the undersigned practitioner by telephone if the Examiner has any questions or suggestions concerning this amendment, the application, or allowance of any claims thereof.

I hereby certify under 37 CFR 1.8 that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office on the date of signature shown below.

Respectfully submitted,
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